## CLAIMS

What is claimed is:

1. A method comprising:

electrically connecting a first kicker device to a first drain bias for a first non-volatile memory cell, wherein said first kicker device comprises a high performance transistor;

enabling said first kicker device; and

pulling a voltage of said first drain bias towards a voltage potential of a supply source.

2. The method of claim 1, wherein said first non-volatile memory cell is a flash memory cell.

3. The method of claim 1, wherein said high performance transistor is a p-channel semiconductor device.

4. The method of claim 1, wherein said first kicker device is enabled prior to sensing the contents of said first non-volatile memory cell.

5. The method of claim 1, wherein:

said first non-volatile memory cell is included in a data array;

a second kicker device is electrically connected to a second drain bias for a second non-volatile memory cell;

said second non-volatile memory cell is included in a reference array; and

said first kicker device and said second kicker device pull a voltage of a sense node for said first non-volatile memory cell and a voltage of a reference node for said second non-volatile memory cell towards the same voltage potential.

6. The method of claim 1, wherein said first drain bias comprises a cascode amplifier.

7. A kicker for a non-volatile memory drain bias circuit, comprising:

a high performance transistor, wherein a first terminal of said high performance transistor receives a voltage from a supply voltage and a second terminal of said high performance transistor provides a voltage to said non-volatile memory drain bias circuit; and

an enable signal, wherein said enable signal activates said high performance transistor.

8. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said non-volatile memory drain bias circuit provides the drain bias for a flash memory cell.

9. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said high performance transistor is a p-channel semiconductor device.

10. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said kicker pulls the voltage of a node towards the voltage potential of a supply source.

11. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said kicker is enabled prior to sensing the contents of a first non-volatile memory cell.

12. The kicker for a non-volatile memory drain bias circuit of claim 11, wherein:
said first non-volatile memory cell is included in a data array;
a second kicker is electrically connected to a second drain bias for a second non-volatile memory cell;
said second non-volatile memory cell is included in a reference array; and
said kickers pull a sense node for said first non-volatile memory cell and a reference node for said second non-volatile memory cell towards the same voltage potential.

13. The kicker for a non-volatile memory drain bias circuit of claim 7, wherein said non-volatile memory drain bias circuit comprises a cascode amplifier.

14. A non-volatile memory device, comprising:
a first drain bias circuit for a first memory cell;
a first kicker circuit for said first drain bias circuit, wherein said first kicker circuit comprises a high performance transistor and wherein said first kicker circuit pulls the voltage of a node towards a voltage potential of a supply source.

15. The non-volatile memory device of claim 14, wherein said non-volatile memory device is a flash memory device.

16. The non-volatile memory device of claim 14, wherein said high performance transistor is a p-channel device.

17. The non-volatile memory device of claim 14, wherein said first kicker circuit acts as a low resistance path to said supply voltage and said first kicker circuit charges the bitline for said first memory cell.

18. The non-volatile memory device of claim 14, wherein said first kicker circuit is enabled prior to sensing the contents of said first memory cell.

19. The non-volatile memory device of claim 14, further comprising:
a second drain bias circuit for a second memory cell; and
a second kicker circuit for said second drain bias circuit, wherein:
said first memory cell is included in a data array;
said second memory cell is included in a reference array; and
said first kicker circuit and said second kicker circuit pull a sense node for said first memory cell and a reference node for said second memory cell towards the same voltage potential.

20. The non-volatile memory device of claim 14, wherein said first drain bias circuit comprises a cascode amplifier.

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